

i Cover Sheet

Department of Physics

Examination paper for TFY4185 Measurement Technique / Måleteknikk

Examination date: 13 August 2021

Examination time (from-to): 09:00-13:00

Permitted examination support material: All support material is allowed

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Technical support during examination: Orakel support services:

Link: innsida.ntnu.no/wiki/-/wiki/English/Orakel+Support+Services

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OTHER INFORMATION

Only contact academic contact in case of errors or insufficiencies in the question set.

Saving: Answers written in Inspira are automatically saved every 15 seconds. If you are working in another program remember to save your answer regularly.

Cheating/Plagiarism: The exam is an individual, independent work. *Examination aids are permitted.* All submitted answers will be subject to plagiarism control. Read more about cheating and plagiarism here: innsida.ntnu.no/wiki/-/wiki/English/Cheating+on+exams

Notifications: If there is a need to send a message to the candidates during the exam (e.g. if there is an error in the question set), this will be done by sending a notification in Inspira. A dialogue box will appear. You can re-read the notification by clicking the bell icon in the top right-hand corner of the screen. All candidates will also receive an SMS to ensure that nobody misses out on important information. Please keep your phone available during the exam.

Weighting: *Each correct answer is weighted 4 points. Each incorrect or blank answer is 0 points. Answers are not necessarily exact. You must choose the best or closest answer.*

ABOUT SUBMISSION

Your answers will be submitted automatically when the examination time expires and the test closes, if you have answered at least one question. This will happen even if you do not click "Submit and return to dashboard" on the last page of the question set. You can reopen and edit your answer as long as the test is open. If no questions are answered by the time the examination time expires, your answers will not be submitted.

Withdrawing from the exam: If you wish to submit a blank test/withdraw from the exam, go to the menu in the top right-hand corner and click "Submit blank". This **can not** be undone, even if the test is

still open.

Accessing your answer post-submission: You will find your answer in Archive when the examination time has expired.

i Information about the exam

Other information:

All questions are 4 points for correct answer, 0 for incorrect or blank answer

Answers may not be exact, so **choose the best answer**

The course will be graded pass/fail (bestått/ikke bestått).

This year, in accordance with advice from the NTNU administration, the pass level for the course will be set at the E-level or above. That is, 41% or better will be a pass. You will have to pass both the laboratory section as well as this exam to receive a pass for the course.

i Logic Help Sheet

Help pages

Boolean identities

AND function

$$\begin{aligned}0 \cdot 0 &= 0 \\0 \cdot 1 &= 0 \\1 \cdot 0 &= 0 \\1 \cdot 1 &= 1 \\A \cdot 0 &= 0 \\0 \cdot A &= 0 \\A \cdot 1 &= A \\1 \cdot A &= A \\A \cdot A &= A \\A \cdot \bar{A} &= 0\end{aligned}$$

OR function

$$\begin{aligned}0 + 0 &= 0 \\0 + 1 &= 1 \\1 + 0 &= 1 \\1 + 1 &= 1 \\A + 0 &= A \\0 + A &= A \\A + 1 &= 1 \\1 + A &= 1 \\A + A &= A \\A + \bar{A} &= 1\end{aligned}$$

NOT function

$$\begin{aligned}\bar{0} &= 1 \\ \bar{1} &= 0 \\ \overline{\bar{A}} &= A\end{aligned}$$

Boolean laws

Commutative law

$$\begin{aligned}AB &= BA \\A + B &= B + A\end{aligned}$$

Absorption law

$$\begin{aligned}A + AB &= A \\A(A + B) &= A\end{aligned}$$

Distributive law

$$\begin{aligned}A(B + C) &= AB + AC \\A + BC &= (A + B)(A + C)\end{aligned}$$

De Morgan's law

$$\begin{aligned}\overline{A + B} &= \bar{A} \cdot \bar{B} \\ \overline{A \cdot B} &= \bar{A} + \bar{B}\end{aligned}$$

Associative law

$$\begin{aligned}A(BC) &= (AB)C \\A + (B + C) &= (A + B) + C\end{aligned}$$

Note also

$$\begin{aligned}A + \bar{A}B &= A + B \\A(\bar{A} + B) &= AB\end{aligned}$$

Function	Symbol	Alternative symbol	Boolean expression	Truth table															
Buffer			$B = A$	<table><tr><th>A</th><th>B</th></tr><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></table>	A	B	0	0	1	1									
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NOT			$B = \overline{A}$	<table><tr><th>A</th><th>B</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>	A	B	0	1	1	0									
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AND			$C = A \cdot B$	<table><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	A	B	C	0	0	0	0	1	0	1	0	0	1	1	1
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OR			$C = A + B$	<table><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	A	B	C	0	0	0	0	1	1	1	0	1	1	1	1
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Function	Symbol	Alternative symbol	Boolean expression	Truth table															
NAND			$C = \overline{A \cdot B}$	<table><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	A	B	C	0	0	1	0	1	1	1	0	1	1	1	0
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NOR			$C = \overline{A + B}$	<table><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	A	B	C	0	0	1	0	1	0	1	0	0	1	1	0
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Exclusive OR			$C = A \oplus B$	<table><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	A	B	C	0	0	0	0	1	1	1	0	1	1	1	0
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Exclusive NOR			$C = \overline{A \oplus B}$	<table><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	A	B	C	0	0	1	0	1	0	1	0	0	1	1	1
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i Transistor Help Sheet

BJT parameters for common emitter configuration (subscript _e)

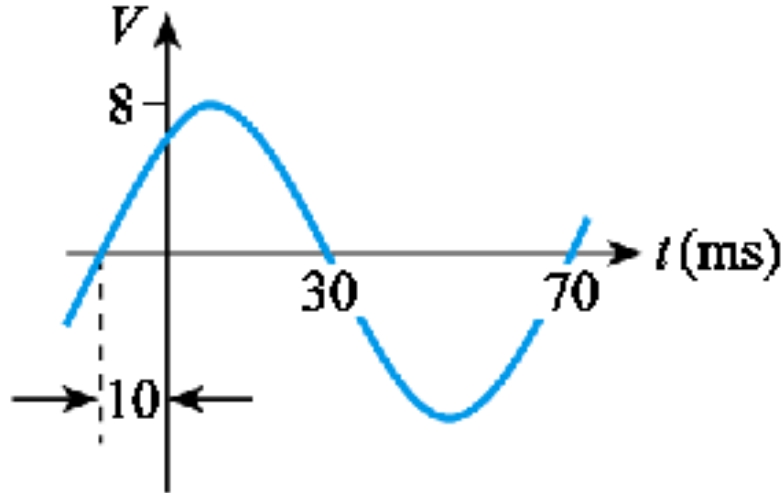
other subscripts: Input_i Output_o Forward_f Reverse_r

h_{FE}	DC gain	I_C / I_B	
h_{fe}	AC gain	i_c / i_b	$h_{FE} \approx h_{fe}$ (mostly)
g_m	Transconductance	$\Delta I_C / \Delta V_{BE} = i_c / v_{be}$	$\sim 40 \cdot I_C \approx 40 \cdot I_E$
h_{ie}	Small signal input resistance	$\Delta V_{BE} / \Delta I_B = v_{be} / i_b$	$\sim 1 / (40 \cdot I_B) \Omega \approx h_{fe} / (40 \cdot I_C)$
h_{oe}	Output admittance ($1/r_o$) where r_o = Slope in the active region	$\Delta I_C / \Delta V_{CE} = i_c / v_{ce}$	
r_e	Emitter resistance	$\Delta V_{BE} / \Delta I_C = v_{be} / i_c = 1/g_m$	$\approx v_{be} / i_e$ that is, $h_{ie} = h_{fe} \cdot r_e$
h_{re}	Early effect (V_{CE} affects bias V_{BE})	$\Delta V_{CE} / \Delta V_{BE}$	

$h_{FE} = \frac{I_C}{I_B}$ $I_E = I_C + I_B = (h_{FE} + 1) \cdot I_B$ <i>but because $h_{FE} \gg 1$,</i> $I_E \approx h_{FE} \cdot I_B = I_C$	$I_B = I_{BS} \cdot e^{40 \cdot V_{BE}} \quad \text{where } I_{BS} \text{ is constant}$ $I_C = h_{FE} \cdot I_B = h_{FE} \cdot I_{BS} \cdot e^{40 \cdot V_{BE}}$ $g_m = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{dI_C}{dV_{BE}} = 40 \cdot h_{FE} \cdot I_{BS} \cdot e^{40 \cdot V_{BE}}$ $g_m = \quad \quad \quad = 40 \cdot I_C \approx 40 \cdot I_E$
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1 TFY4185 2021S AC Fundamentals 1

Which of the following equations describes the waveform shown here?



Select one alternative:

- ☒ $v = 8 \sin (79t + \pi / 4)$
- ☐ $v = 8 \sin (79t - \pi / 4)$
- ☐ $v = 8 \sin (90t + \pi / 4)$
- ☐ $v = 8 \sin (90t - \pi / 4)$

Maximum marks: 4

Clearly a sinusoid with an amplitude of 8. It crosses zero at -10, 30 and 70 ms, making it a period of $T=80$ ms. The time factor in the sinusoid is $\omega \cdot t = 2\pi \cdot t / T$, or in this case $(78.5 \text{ radians/s}) \cdot t$. Now, when $t=0$, the sine has already risen from 0 and is positive, indicating that the phase factor must be positive. While it might be difficult to judge $0.707 \cdot 8$ amplitude units, the only choices are $\pm \pi/4$, and at $t=0$, a $-\pi/4$ would yield a negative number. Thus, the correct answer is $8 \cdot \sin \left(78.5 \cdot t + \frac{\pi}{4} \right)$.

2 TFY4185 2021S AC Power 2

The voltage across a component is measured as 80 V r.m.s. and the current through it is 4 A r.m.s. If the current leads the voltage by 20° what is the apparent power in the component?

Select one alternative:

- ☐ 109 VA
 - ☐ 116 VA
 - ☐ 301 VA
 - ☒ 320 VA
- The Apparent power is $S = V_{rms} I_{rms}$ VA, and the power factor is the cosine of the phase angle, ϕ , between voltage and current. The Active power is then the apparent power times the cosine factor, or $P = S \cos(\phi)$ W. Here the Apparent power is $80 \cdot 4 = 320$ VA, and the power factor is $\cos(20^\circ) = 0.94$. This gives an Active power of 300.7 W

Maximum marks: 4

3 TFY4185 2021S BJT 1

In a bipolar junction transistor the base region is made very thin so that:

Select one alternative:

- ☐ the base can be easily fabricated
- ☐ the electric field gradient in base is high
- ☒ recombination in base region is minimum
- ☐ the base can be easily biased

The point of a transistor is to take electrons from the emitter and pass them to the collector, completing the circuit, but to be able to stop that flow with a low current/voltage to the base that sets up a potential barrier. When the transistor is "on", you do want those negative electrons to pass through the base to the collector without recombining with positive holes in the base. Thus, you make the base thin in order to allow those electrons to flow without recombining.

Maximum marks: 4

4 TFY4185 2021S BJT 5

When bi-polar transistors are used in digital circuits they usually operate in the:

Select one alternative:

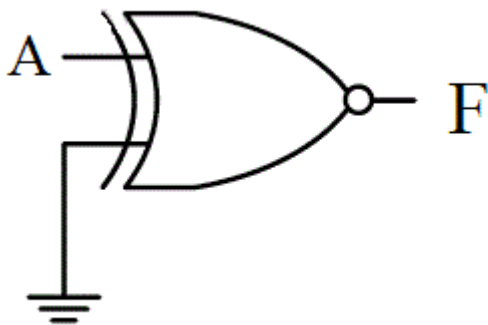
- ☐ Breakdown region
- ☐ Linear region
- ☐ Active region
- ☒ Saturation and cutoff regions

Operating a transistor in a digital device one wants to have the transistor either fully on or fully off. Thus, we operate a BJT transistor in the saturation or cut-off region.

Maximum marks: 4

5 TFY4185 2021S Logic Combinational 6

The output of the logic gate in figure is



Select one alternative:

- ☐ A
- ☐ 0
- ☒ $\bar{A}$
- ☐ 1

Maximum marks: 4

6 TFY4185 2021S Op Amp 5

The ideal Op–Amp has the following characteristics:

Select one alternative:

☐ $R_i = \infty, A = \infty, R_o = \infty$

☒ $R_i = \infty, A = \infty, R_o = 0$

☐ $R_i = 0, A = \infty, R_o = \infty$

☐ $R_i = 0, A = \infty, R_o = 0$

An ideal operational amplifier would have infinite input impedance, R_i , so as not to load the input circuitry. It would have an infinite openloop gain, A , to make it controllable by the external feedback components. Finally, it would have no output impedance, R_o , so that any voltage created by the op-amp would be transferred to the external circuitry without dividing it.

Maximum marks: 4

7 TFY4185 2021S Op amp 2

What does negative feedback derived from the output voltage do to a voltage amplifier?

Select one alternative:

☐ It does not affect impedance or bandwidth.

☐ It increases the input and output impedances.

☒ It increases the input impedance and bandwidth.

☐ It decreases the output impedance and bandwidth.

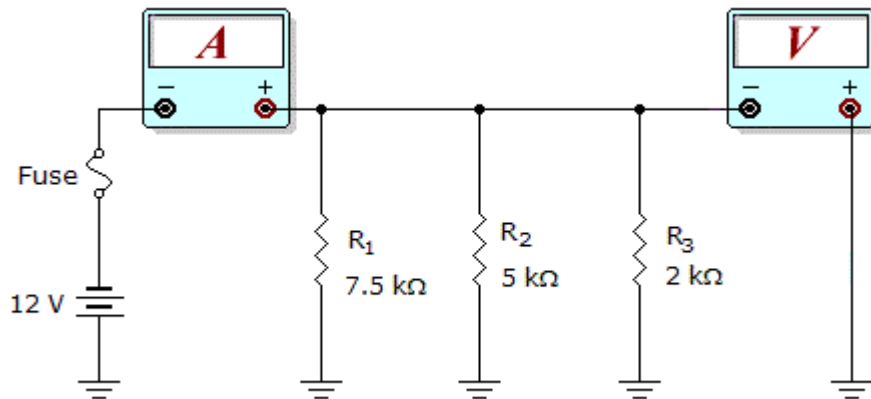
Negative feedback will decrease the gain from the open-loop gain. However since the gain-bandwidth product is constant, this will increase the bandwidth.

Op-amps using negative feedback derived from the output voltage will tend toward an ideal op-amp, with input impedances and output impedances tending toward an ideal amplifier by factors of $1+AB$, the product of the open-loop gain, A , times the closed loop gain, B .

Maximum marks: 4

8 TFY4185 2021S Resistance 17

What would meter readings of $I = 10.0 \text{ mA}$ and $V = 12 \text{ V}$ indicate about the circuit in the circuit given below?



Select one alternative:

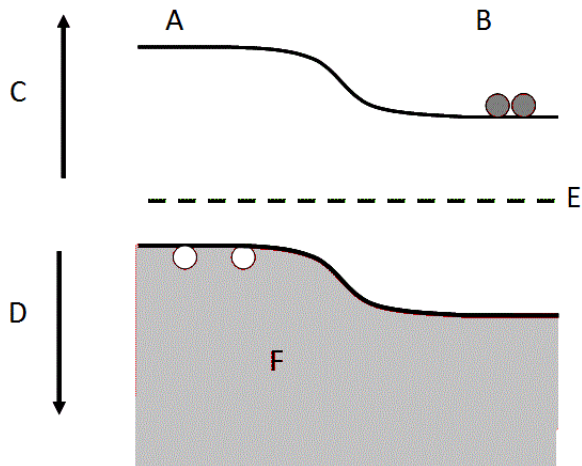
- ☐ R_2 is open
- ☐ R_3 is shorted
- ☐ R_1 is open
- ☐ R_3 is open
- ☒ There is nothing wrong with the circuit, it is functioning normally
- ☐ The fuse is open

Here we have to remember that the voltage across a set of resistors in parallel is the same. Thus, the 12 V tells you that none of the resistors are shorted otherwise it would be 0 V (the voltmeter would be connected to ground on both sides). However one could still be open. The equivalent resistance of the parallel network would be the voltage, 12V, divided by the current, 10 mA = 1.2 k Ω . When we calculate the equivalent resistance of the network, we find that it is 1.2 k Ω , so there is nothing wrong with the circuit.

Maximum marks: 4

9 TFY4185 2021S Semiconductors and diodes 4

The diagram below shows a p-n junction that is not connected to an external circuit. Enter the letter labelling the n-type material.



Select one alternative:

- ☐ A
 - ☒ B
 - ☐ C
 - ☐ D
 - ☐ E
 - ☐ F
- Since electrons are the more mobile charge carriers, the potential energy diagrams are set up with the potential energy of electrons increasing in the upward direction (in the direction of C). Once the junction is formed, the free electrons in the n-type material near the junction diffuse across the junction and re-combine with the excess positive holes in the p-type material. This leaves a net positive charge on the n-side of the junction (lower potential energy for electrons) and a net negative charge on the p-side (higher potential energy for electrons). Thus, electrons are given energy to promote them from the lower electron energy valence band, F, into the higher electron potential energy conduction band A&B. However, the electrons in the conduction band will drift to a lower electron potential energy across the junction (towards the positive side of the junction), B. **This positive side of the junction is, as we said above, the n-type material**

Maximum marks: 4

10 TFY4185 2021S Semiconductors and diodes 6

The diffusion potential across an unbiased p-n junction

Select one alternative:

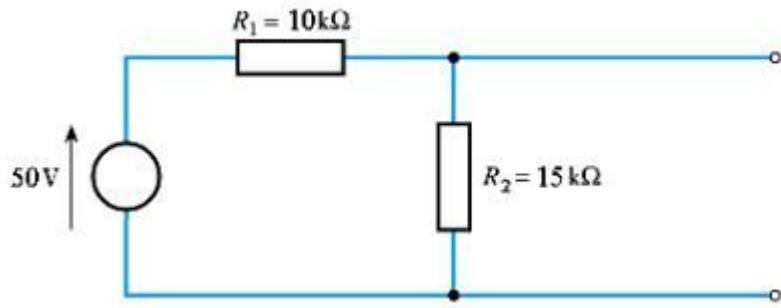
- ☐ does not depend on doping concentrations
- ☐ decreases with increasing doping concentration
- ☐ increases with decreasing band gap
- ☒ increases with increased doping concentrations

The diffusion current is the current of the free charges in the doped material neutralizing each other across the junction to create the depletion region and set up the electric field. The higher the doping level the more free charges in the material and the higher the diffusion current.

Maximum marks: 4

11 TFY4185 2021S Solving Circuits 3

Determine the short-circuit current of the following circuit.



Select one alternative:

☐ 2 mA

☒ 5 mA

Short out the terminals (connect a wire across them), and the current will avoid R_2 and flow through the wire. Thus the current will be $10\text{ V} / 10\text{ k}\Omega = 5\text{ mA}$.

☐ 3.33 mA

☐ 6.67 mA

Maximum marks: 4

12 TFY4185 2021S AC Power 4

The voltage across a component is measured as 80 V r.m.s. and the current through it is 4 A r.m.s. If the current leads the voltage by 20° what is the active power in the component?

Select one alternative:

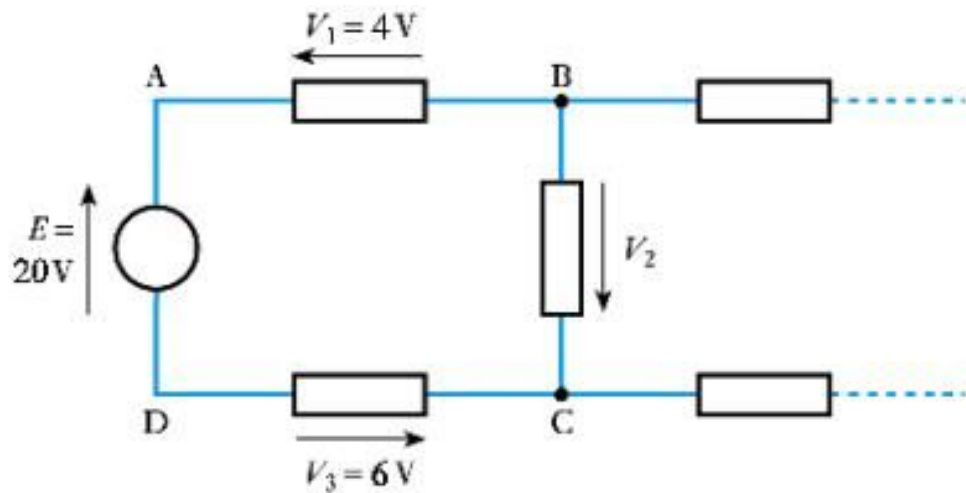
- ☐ 116 W
- ☒ 301 W

The Apparent power is $S = V_{rms} \cdot I_{rms}$ VA, and the power factor is the cosine of the phase angle, ϕ , between voltage and current. The Active power is then the apparent power times the cosine factor, or $P = S \cdot \cos(\phi)$ W. Here the Apparent power is $80 \cdot 4 = 320$ VA, and the power factor is $\cos(20^\circ) = 0.94$. This gives an Active power of 300.7 W
- ☐ 109 W
- ☐ 320 W

Maximum marks: 4

13 TFY4185 2021S Solving Circuits 1

Calculate the voltage V_2 in the following circuit.



Select one alternative:

☐ 12

☐ 10

☒ -10

☐ 10

By convention, we assign the voltage so that the arrow points to the high potential end and we assign it a positive value. If we are not sure, one can assign an arbitrary direction, but if the solution comes out negative, or if it is pointing to the low potential, it will have a negative value. This tells you that the high potential end is actually at the tail of the arrow as we have drawn it!

So, here we have a voltage source of $E = 20\text{ V}$. That means its potential at point A is 20 V higher than the potential at point D. Now for convenience we will take point D, which is the reference point for all the potentials shown, to be at 0 V (remember that potential needs a reference point). Now, potential at point A is $V_A = 20\text{ V}$ above the potential at point D, where $V_D = 0\text{ V}$, and the arrow E points to the higher potential and is assigned a positive value.

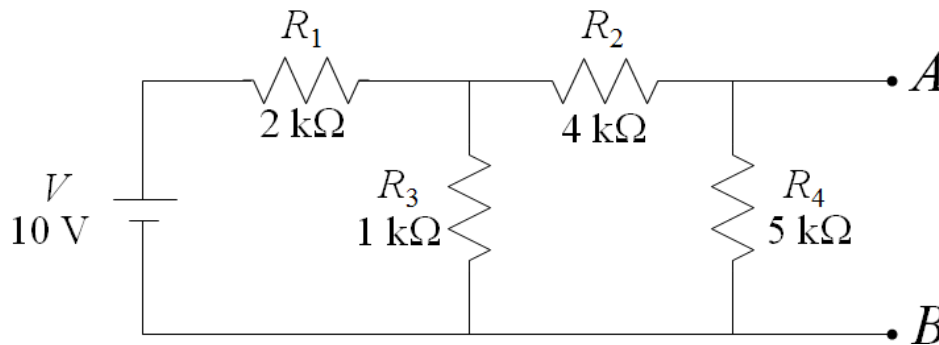
From point A to B, the potential drops $V_1 = 4\text{ V}$ across the resistor. Thus, the point B is at a lower potential $V_B = 20 - 4 = 16\text{ V}$. Note that the voltage arrow V_2 is pointing to the higher potential end and V_2 is assigned a positive value. From point D to C, we see that the potential difference across the resistor is $V_3 = 6\text{ V}$. Now point D is at 0 V, and we know that point B is at 16 V, so point C must be at higher potential than point D by 6 V. Thus, point C is at $V_C = 6\text{ V}$, and again V_3 is pointing to the high potential end and is given a positive sign.

That means that there is a potential difference from $V_B = 16\text{ V}$ to $V_C = 6\text{ V}$, or a 10 V potential drop with $V_B > V_C$. Unfortunately, our choice of direction for V_2 is pointing toward the low potential end. Thus, we have that $V_2 = -10\text{ V}$, to warn it is pointing to the low potential end.

Maximum marks: 4

14 TFY4185 2021S Thevenin Norton 1

In the circuit below, what is the Thevenin voltage and resistance?



Select one alternative:

- ☐ 1.72 V and 666 Ω
- ☐ 3.10 V and 2.41 $\text{k}\Omega$
- ☐ 3.10 V and 9.90 $\text{k}\Omega$
- ☒ 1.72 V and 2.41 $\text{k}\Omega$

If we short out the power supply, we can look at the equivalent resistance from A to B. This will be the Thevenin resistance. If we start at B, we find that R_1 , R_3 and R_4 are all connected together at B. The upper end of R_1 and R_3 are connected together, putting them in parallel. This parallel junction is connected to R_2 , and thus the parallel pair $R_1//R_3$ is in series with R_2 . The upper end of R_2 is connected to the upper end of R_4 at terminal A, and so R_4 is in parallel with $R_1//R_3+R_2$.

We can break it down and calculate the parallel pair R_1 and R_3 as $R_{eq1} = R_1 * R_3 / (R_1 + R_3)$, or substituting in values, we get $R_{eq1} = 666.7\Omega$

This is in series with R_2 , giving a $R_{eq2} = R_{eq1} + R_2 = 4.66\text{ k}\Omega$. Finally, this R_{eq2} is in parallel with R_4 , giving the total, Thevenin resistance $R_{th} = R_{eq2} * R_4 / (R_{eq2} + R_4)$. Again substituting in values gives $R_{th} = 2.41\text{ k}\Omega$

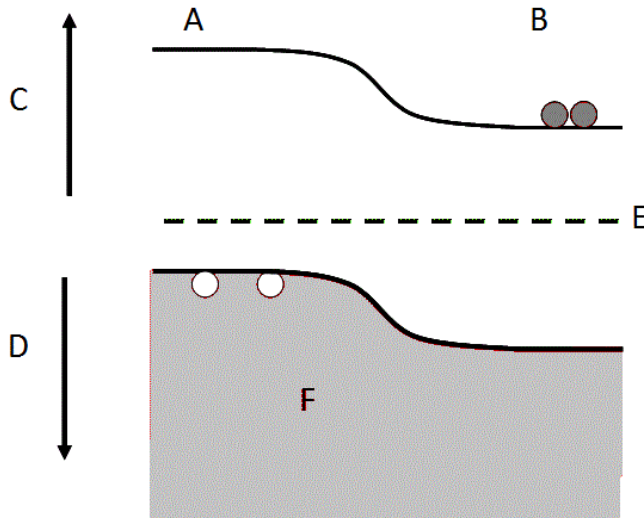
To get the voltage across A and B, the Thevenin voltage, we have to put the power supply back in the circuit. Now we need to calculate the total current, which means we need to look at the equivalent resistance seen by the power supply. From the figure, we can see that this is R_2 and R_4 in series, and this series resistance in parallel with R_3 . Lastly, R_1 is in series with the parallel pair. So we have $R_1 + R_3 // (R_2 + R_4)$. The series of R_2 and R_4 is 9 $\text{k}\Omega$, and this is in parallel with $R_3 = 1\text{ k}\Omega$. So this would be $9 * 1 / (9 + 1)\text{ k}\Omega$, or 0.9 $\text{k}\Omega$. Finally we add the series resistance of $R_1 = 2\text{ k}\Omega$, and we get an equivalent resistance as seen by the power supply of $R_{tot} = 2.9\text{ k}\Omega$.

Finally, the current is $I = V / R_{tot} = 10\text{V} / 2.9\text{ k}\Omega = 3.45\text{ mA}$. The voltage after R_1 is just $10\text{V} - I * R_1$, or $10\text{V} - 6.89\text{V} = 3.1\text{V}$. Now, this voltage, V_p , is divided across the two resistors R_2 and R_4 , and the voltage across R_4 is $V_p * R_4 / (R_4 + R_2)$. This is just the voltage divider equation. So $V_4 = V_{th} = 3.1 * 5 / (5 + 4)$, or $V_{th} = 1.72\text{ V}$

Maximum marks: 4

15 TFY4185 2021S Semiconductors and diodes 2

The diagram below shows a p-n junction that is not connected to an external circuit. Enter the letter labelling the Valence band.



Select one alternative:

- ☐ A Since electrons are the more mobile charge carriers, the potential energy diagrams are set up with the potential energy of electrons increasing in the upward direction (in the direction of C). Once the junction is formed, the free electrons in the n-type material near the junction diffuse across the junction and re-combine with the excess positive holes in the p-type material. This leaves a net positive charge on the n-side of the junction (lower potential energy for electrons) and a net negative charge on the p-side (higher potential energy for electrons). Thus, electrons are given energy to promote them from the lower electron energy valence band, F, into the higher electron potential energy conduction band A&B. However, the electrons in the conduction band will drift to a lower electron potential energy across the junction (towards the positive side of the junction), B. This positive side of the junction is, as we said above, the n-type material
- ☐ B
- ☐ C
- ☐ D
- ☐ E
- ☒ F

Maximum marks: 4

16 TFY4185 2021S Reactance 3

What is the capacitive reactance if $I = 1$ amp, $V = 2$ volts, $C = 5$ F, and frequency = 10 Hz?

Select one alternative:

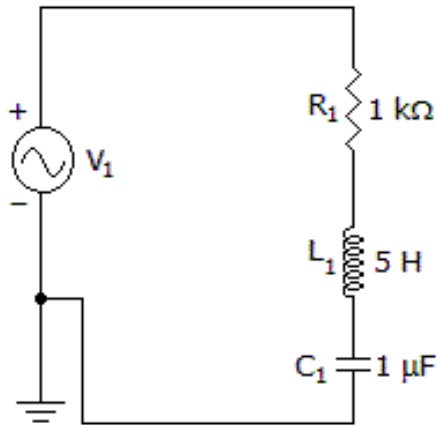
- ☐ 0.02 Ω
- ☐ 0.5 Ω
- ☒ 0.003 Ω
- ☐ 0.2 Ω

Capacitive reactance is defined as $X_c = \frac{1}{\omega \cdot C}$, where ω (rad/s) = $2\pi \cdot f$ (Hz). Here we have $f=10$ Hz, giving $\omega=62.8$ rad/s, and with a capacitance of $C= 5$ F, $X_c = 1/(62.8 \cdot 5) = 0.003 \Omega$

Maximum marks: 4

17 TFY4185 2021S RLC and Transients 6

What is the resonant frequency of the circuit below?



Select one alternative:

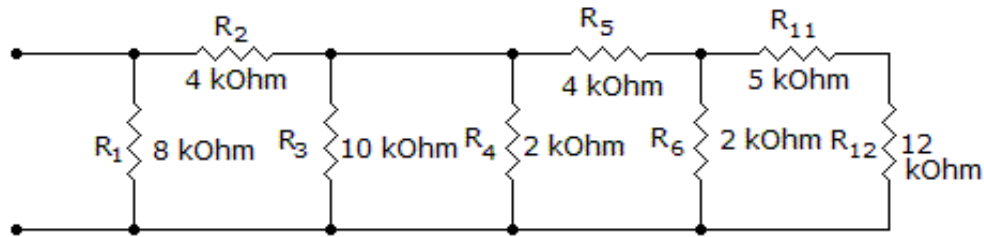
- ☐ 32 Hz
- ☒ 71 Hz
- ☐ 200 Hz
- ☐ 447 Hz

The resonant frequency of an R-L-C series circuit is $\omega = \frac{1}{\sqrt{L \cdot C}}$. So, for $L=5\text{ H}$, and $C=1 \times 10^{-6}\text{ F}$, we have that $\omega=447\text{ radians/s}$. Unfortunately the units of the answer are in Hz. Thus, since $f\text{ (Hz)} = \omega/(2\pi)$, the frequency $f = 71.2\text{ Hz}$

Maximum marks: 4

18 TFY4185 2021S Resistance 12

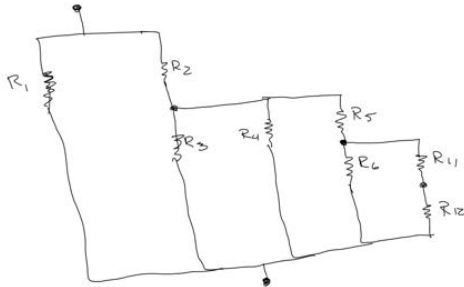
What is the total resistance of the circuit below?



Select one alternative:

- ☐ 5.2 k Ω
- ☐ 2.2 k Ω
- ☐ 4.2 k Ω
- ☒ 3.2 k Ω

Tracing through the top terminal through the chain, we see can draw the circuit like this:



Maximum marks: 4

Now, R_{11} and R_{12} are in series with each other, and the series pair is in parallel with R_6 :

$$Req1 = (R_{11} + R_{12}) // R_6$$

This $Req1$ is in series with R_5 , and this series pair is in parallel with R_4 :

$$Req2 = (Req1 + R_5) // R_4$$

This $Req2$ is in parallel with R_3 :

$$Req3 = Req2 // R_3$$

This is in series with R_2 , and the series pair of $Req3$ and R_2 are in parallel with R_1 :

$$Req = (R_2 + Req3) // R_1$$

Then you just need to remember that series of a and b is $a+b$, and parallel of a and b is $a*b/(a+b)$.

$$Req1 = (5+12)*2/((5+12)+2) = 1.79 \text{ k}\Omega$$

$$Req2 = (1.79+4)*2/((1.79+4)+2) = 1.49 \text{ k}\Omega$$

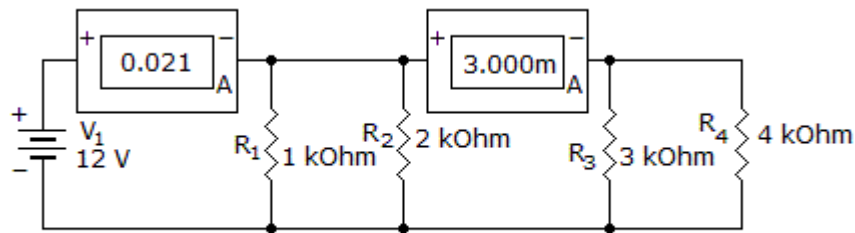
$$Req3 = 1.49*10/(1.49+10) = 1.29 \text{ k}\Omega$$

And

$$Req = (1.29+4)*1/((1.29+4)+1) = 3.19 \text{ k}\Omega$$

19 TFY4185 2021S Resistance 10

Which component is open in the circuit below?



Select one alternative:

☐ R_1

☐ R_2

☐ R_4

☒ R_3

This one is deceptively easy. Here we have a situation where the voltage across all the resistors is the same, 12V. The total current is given as $I_t = 21$ mA, and the current flowing through the parallel pair 3//4 is $I_{34} = 3$ mA. That means the current flowing through the parallel pair 1//2, $I_{12} = I_t - I_{34} = 18$ mA.

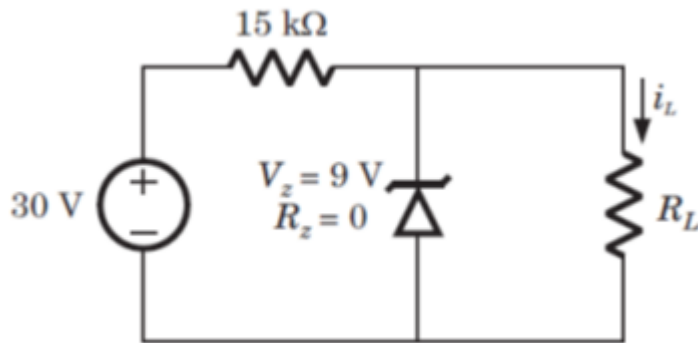
Now, the resistance 1//2 should be $(1 \cdot 2) / (1 + 2) \text{ k}\Omega = 666.7 \text{ }\Omega$. That should be the same as $V / I_{12} = 12\text{V} / 18\text{mA} = 666.7 \text{ }\Omega$. Since it is, that leg is OK and the problem is in the 3//4 leg.

The parallel resistance 3//4 should be $3 \cdot 4 / (3 + 4) \text{ k}\Omega = 1714.3 \text{ }\Omega$. But the current measured flowing through this pair would indicate that the resistance is $R_{34} = 12 \text{ V} / 3 \text{ mA} = 4 \text{ k}\Omega$, the value of R_4 . That means that R_3 is no longer in the circuit and is open.

Maximum marks: 4

20 TFY4185 2021S Zener Diodes

In the voltage regulator circuit in the figure below, what is the maximum load current, i_L , that can be drawn?



Select one alternative:

- ☒ 1.4 mA
 - ☐ 2.3 mA
 - ☐ 2.5 mA
 - ☐ 1.8 mA
- Well, the voltage across the diode is V_d , but to get maximum current across the load, the voltage across the diode, V_d , should be just at the the Zener voltage, V_z , and the diode would be just be at the point of passing current. All the current would go into the load, and increasing the voltage any further would just pass the extra current through the Zener. The voltage across the diode just as it turns on, V_d , is the supply voltage, V_s , divided across the $R_1=15\text{ k}\Omega$ and R_L resistors, or $V_d=V_s \cdot R_L / (R_1+R_L)$. Solving for R_L gives us $R_L=V_d \cdot R_1 / (V_s-V_d)$. The current across the load resistor is just the voltage across the load, V_d , divided by R_L . Or, $I_{\max}=V_d/R_L$. Subtituting in for R_L , and using the fact that $V_d=V_z$, we get

$$I_{\max}=(V_s-V_d)/R_1 = (V_s-V_z)/R_1=(30\text{V}-9\text{V})/15000\ \Omega = 1.4\text{ mA}$$

Maximum marks: 4

21 TFY4185 2021S Semiconductors and diodes

An ideal *pn* junction diode is operating in the forward bias region ($V_d > 0.1 \text{ Volt}$). The change in diode voltage, that will cause a factor of 9 increase in current, is

Select one alternative:

- ☐ 45 mV
 - ☐ 35 mV
 - ☐ 85 mV
 - ☒ 55 mV
- $$I_d = I_s \cdot (\exp(40 \cdot V_d) - 1)$$
- With $V_d = 0.1$, $\exp(40 \cdot 0.1) \gg 1$ so $I_d \approx I_s \cdot \exp(40 \cdot V_d)$
- $$I_{d1}/I_{d2} = 9 \approx \exp(40(V_{d1} - V_{d2}))$$
- $$\ln(I_{d1}/I_{d2}) = \ln(9) \approx 40(V_{d1} - V_{d2})$$
- $$2.19/40 \text{ V} \approx V_{d1} - V_{d2}$$
- $$55 \text{ mV} \approx V_{d1} - V_{d2}$$

Maximum marks: 4

22 TFY4185 2021S FET 2

What are the three terminals of an FET transistor called:

Select one alternative:

- ☐ emitter, base, collector
 - ☒ source, gate, drain
 - ☐ none of the answers are correct
 - ☐ cathode, anode, grid
- On an FET, we have a gate that controls the flow of electrons, a source of electrons, and a drain of electrons. However, in an FET the direction of flow can be source to drain or drain to source depending upon the bias. Fulfilling a similar function on a BJT transistor, we have a base, emitter and collector, where the electrons do flow from the emitter to collector. That terminology, in turn, developed from vacuum tubes (valves) that had a grid, cathode and an anode, where electrons left the cathode toward the anode, but the control of the flow was done with the bias in the grid. Remember, the current flow is in the opposite direction of the electron flow!

Maximum marks: 4

23 TFY4185 2021S Digital Devices 3

As compared to TTL, CMOS logic has

Select one alternative:

- ☐ All answers are correct
- ☐ Higher speed of operation
- ☒ Smaller physical size
- ☐ Higher power dissipation

Maximum marks: 4

24 TFY4185 2021S Logic Combinational 7

Decimal number 9 in Gray code is:

Select one alternative:

- ☐ 1001
- ☒ 1101
- ☐ 111
- ☐ 1100

The point of Gray code is that only one bit changes as the number is increased. It is formed by first counting to 1 in binary

0
1
Then mirroring these numbers

0
1
1
0
Then add a 0 to the initial numbers (0 and 1) and a 1 to the mirrored numbers (1 and 0):

00
01
11
10
Then repeat

00	000	0
01	001	1
11	011	2
10	010	3
10	110	4
11	111	5
01	101	6
00	100	7

and again

000	0000	0
001	0001	1
011	0011	2
010	0010	3
110	0110	4
111	0111	5
101	0101	6
100	0100	7
100	1100	8
101	1101	9
111	1111	10
110	1110	11
101	1101	12
011	1011	13
001	1001	14
000	1000	15

Maximum marks: 4

25 TFY4185 2021S Logic Combinational 4

The output of a logic gate is '1' when all its input are at logic 0. The gate is either

Select one alternative:

- ☒ a NOR or an EX-NOR gate
- ☐ an AND or an EX-OR gate
- ☐ a NAND or an EX-OR gate
- ☐ an OR or an EX-NOR gate

Maximum marks: 4